
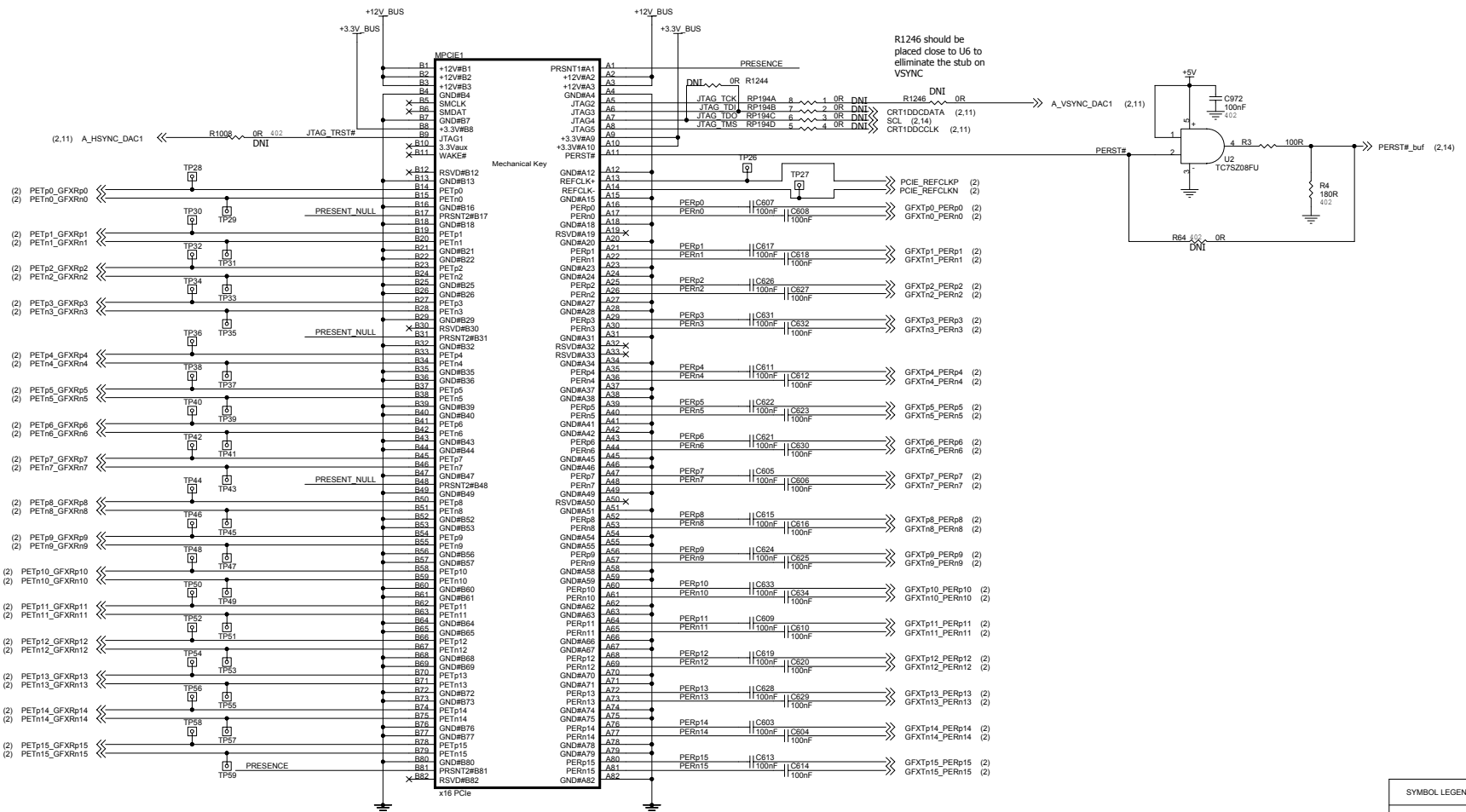


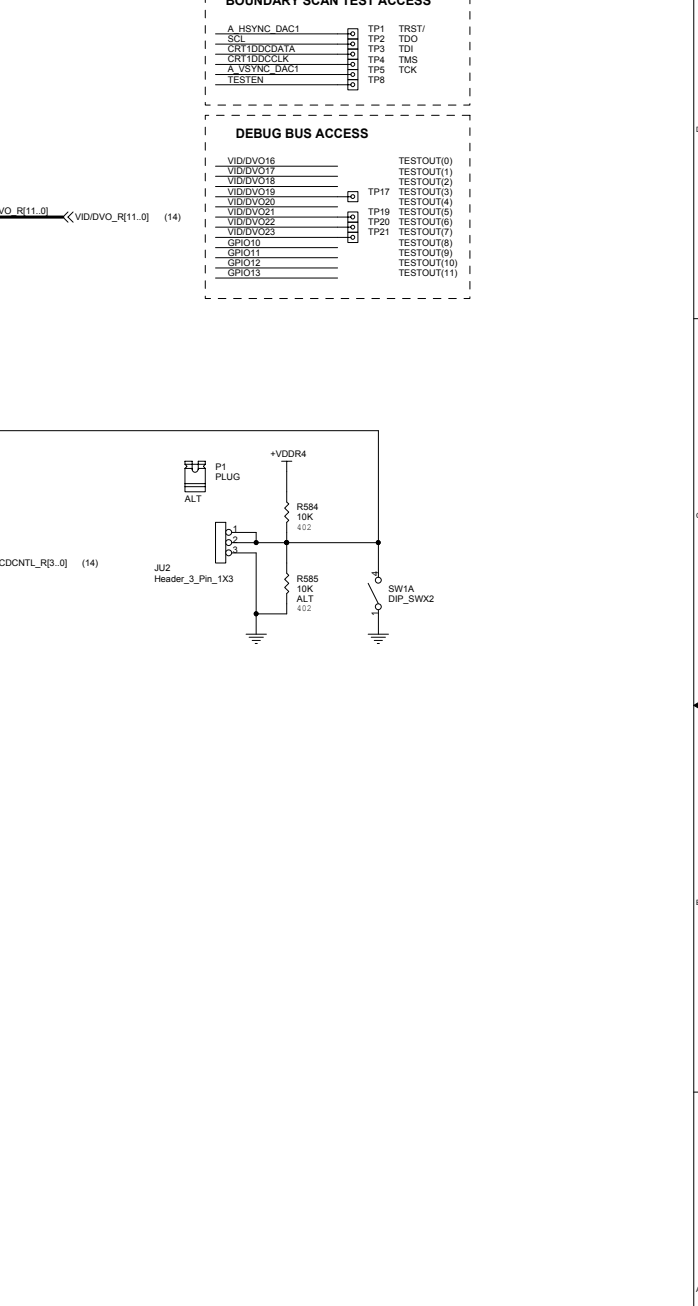
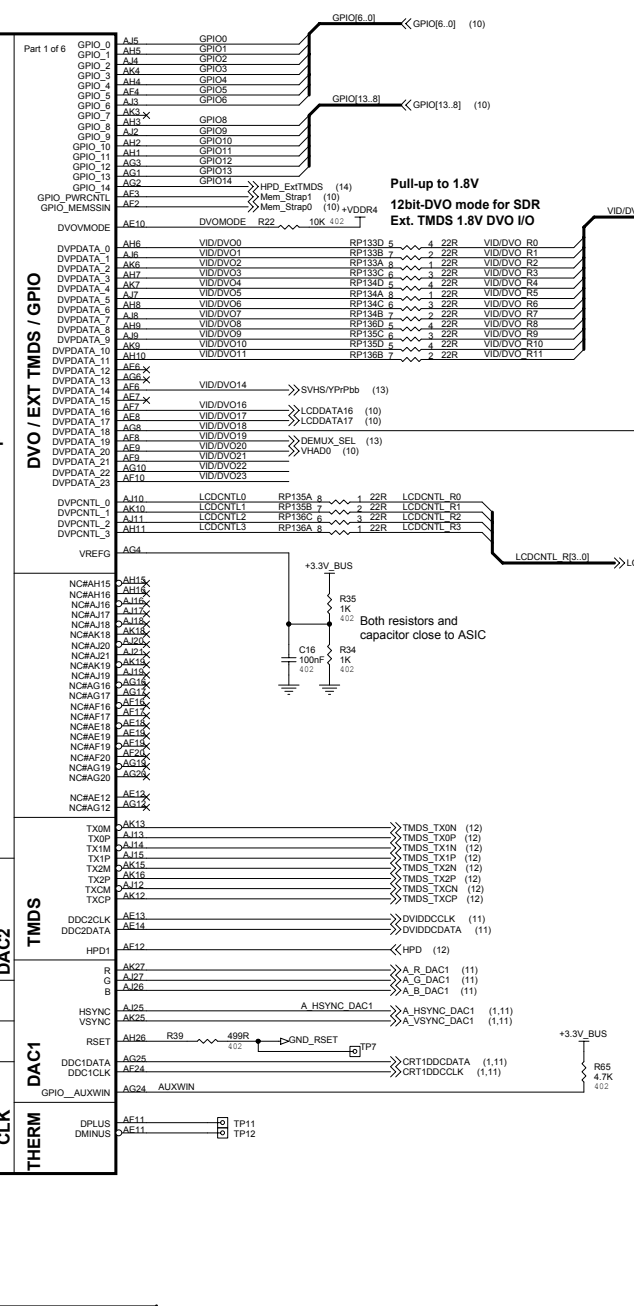
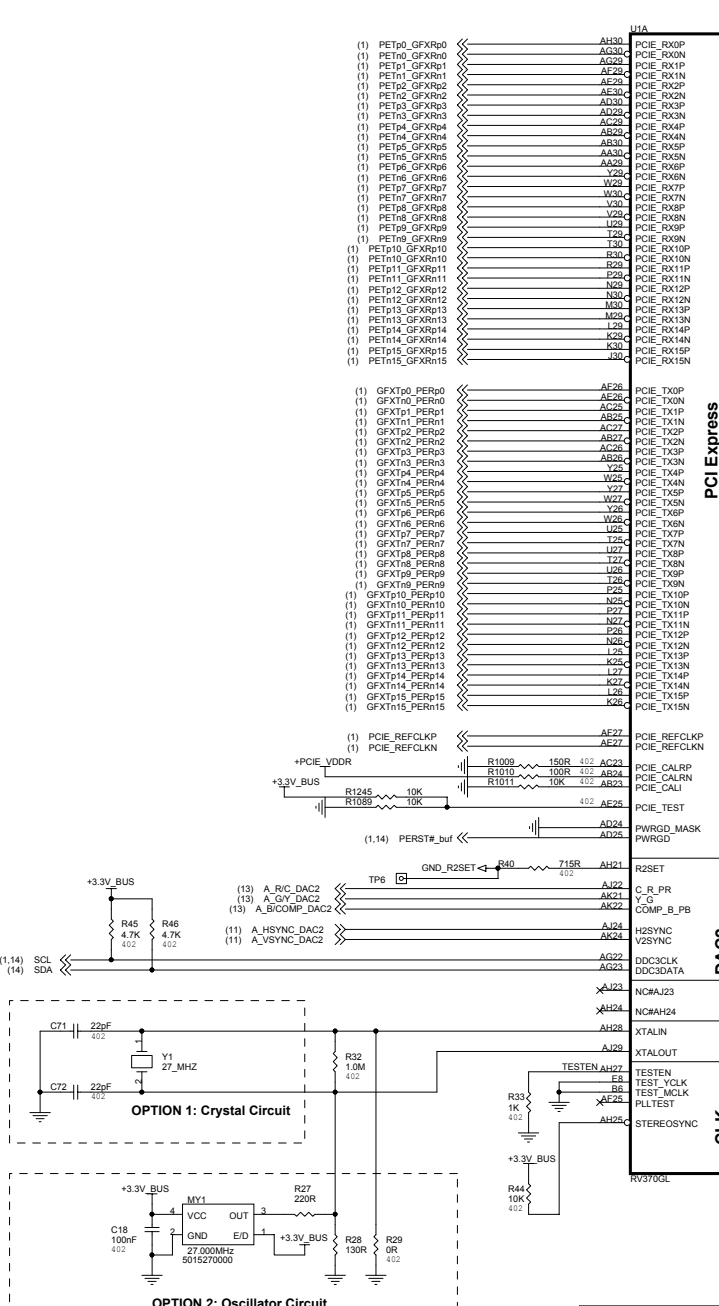


Variant Name>		5	4	3	2	1
		Title PCI-E RV380/370 128M TSOP VO-DMS59			Schematic No. 105-A259xx-00	Date: Thursday, July 15, 2004
REVISION HISTORY						Rev 3
Sch Rev	Date	REVISION DESCRIPTION				
0 00A	2003-09-10	PRELIMINARY BASED ON 105-A181xx-00A and 105-A200xx-00 - Use 402 R and C footprints as preferred - (pg1) Add 0R bypass for PERST#, and use XOR spared gate for buffer - (pg1) Keep only 1 100uF decoupling for +12V_BUS - (pg1) Connect B3 of edge connector directly to +12V_BUS - (pg2) Remove oscillator and change crystal to surface mount - (pg2) Hard pull-down on TEST_Y/MCLK - (pg2) Remove thermal interrupt, no provision for speed controlled fan - (pg2) Remove redundant TPs - (pg2) Pull-up on DVPCNTL_[3:0], remove RageTheater capture ports (VID/DVO[7:0]) - (pg2) DVOMode pull-up to 1.8V, set to 12-bit DVO (1.8V DVO I/O signalling) - (pg3) Memory interface based on A198, remove Channel B - (pg4) Remove power-up diodes - (pg5, 6, 7) Redesigned power regulators - (pg8, 9) Channel A only Series-Terminated TSOP interface (based on A200) - (pg11, 12, 13) Front-end based on Low-Profile VGA/DVI + VO design (based on A200)				
	2003-09-22	- (pg5) Add RC snubber circuit on switching regulator - (pg7) Add R124 for power dissipation				
	2004-01-13	- (Layout) Change to 6 layer - (pg2) Add series resistor for SI1162 DVO and control bus - (pg4) Add C98 and C99 on PCIE_VDDR, remove C980 - (pg5) Remove +Vout_Switcher, add power sequence circuit, remove +A2VDD pull-up on bottom MOSFET - (pg6) Remove MQ31, L12 - (pg6) Replace Q32 with CMPT3904 and add R1044, R1045 for +5V regulator - (pg6) Add R1043 and R1046 for +5V_DDC power and add preferred option of +5V from Opamp regulator, add R146 for PCIE_PVDD18 power sequence - (pg7) Add L4 for +PCIE_PVDD18 to +1.8V - (pg7) Remove Opamp regulator circuits - (pg12) Swapping HPD pins, add +5V_DDC power option - (pg12) Remove TVO signals from DMS-59 connector - (pg14) Change SI164 ext TMDS chip to SI1162				
	2004-01-28	- (pg4) Remove C979, C981, C982, C983, C984 and C985 - (pg13) Change one set of filter capacitor to digital GND - (pg02, 10) Change +VDD_DVO to +VDDR4				
1 00B	2004-04-15	- (pg04) Remove CP2, CP3, CP4, CP5, CP6, CP8, CP9, CP10 and CP11, dual-footprint - (pg05) Add MR357 for power sequencing - (pg06) Remove R6, +5V reg is not required for VESA compliance - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993, dual-footprint - (pg06) Add C800 for stability - (pg07) Remove MC306 and MC308 - (pg11, 12, 13) Remove R991, R992, R993, R997, R998 and R999 for joined ground - (pg12 and 14) Correct R318 and R606 short for HPD - (pg12) Add +5V_VESA and +5V_VESA2 power regulator, remove B21 and F1, add C442 - (pg13) Delete R513 and R514 for EMI, connect TVO shield directly to Chassis GND				
2 00C	2004-06-10	- (Layout) EMI changes Remove int. TMDS ground guard Move ext. TMDS to inner layer Move DVO bus from layer 3 to layer 4 - (pg6) change +VDDC_CT source from +3.3V_BUS - (pg6) change +PCIE_VDDR optional regulator reference from +3.3V_BUS to +PCIE_PVDD18 - (pg14) change TMDS differential pairs termination resistors and capacitors to 402 footprint - (pg14) change AVCC, PVDD, VCC decoupling caps to 402 footprint and add 10uF filtering, spearate PVCC1, PVCC2, AVCC1 and AVCC2. - (pg14) remove R319, R320, R620 and R625 redundant straps				
3 00	2004-07-15	- No schematic change. Layout changes only.				
		5	4	3	2	1

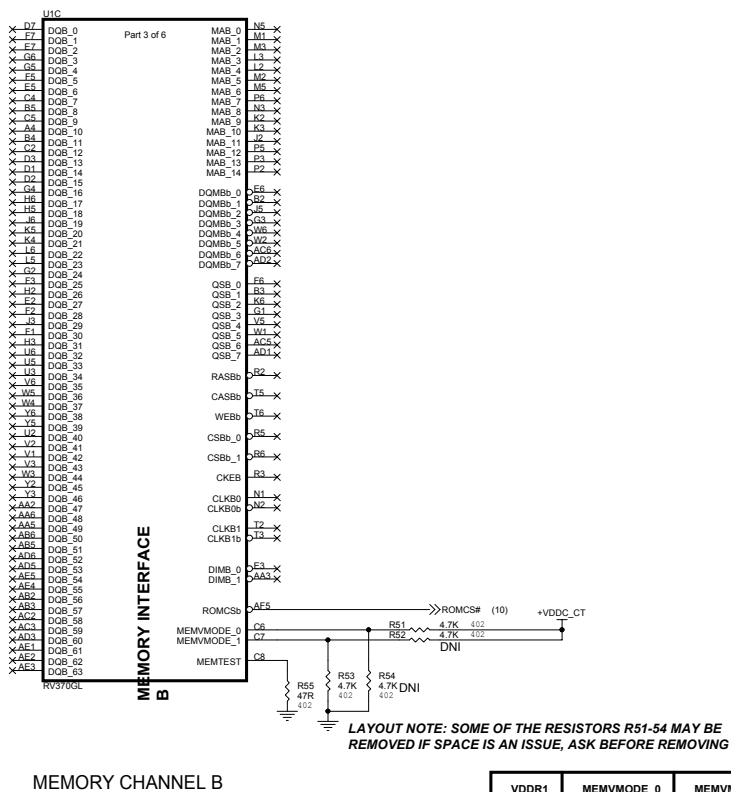
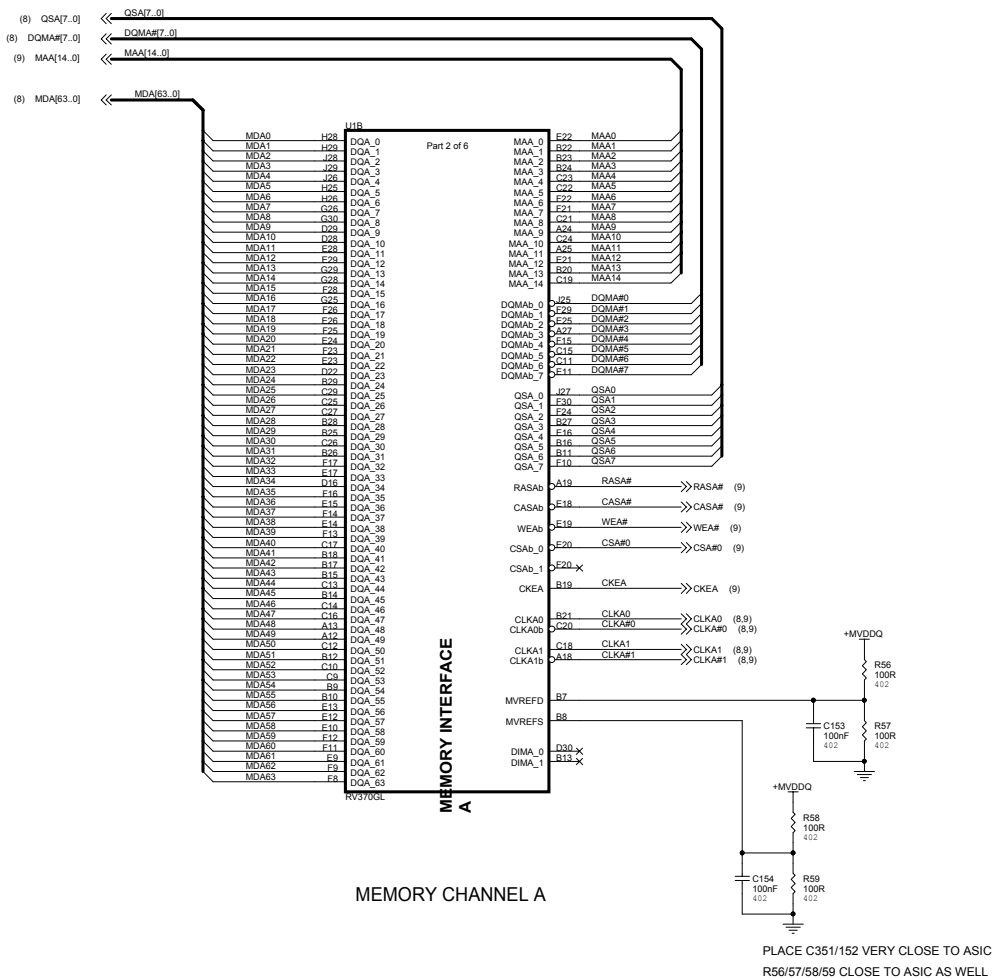
USE 47uF TANTALUM CAPACITOR OR HIGHER



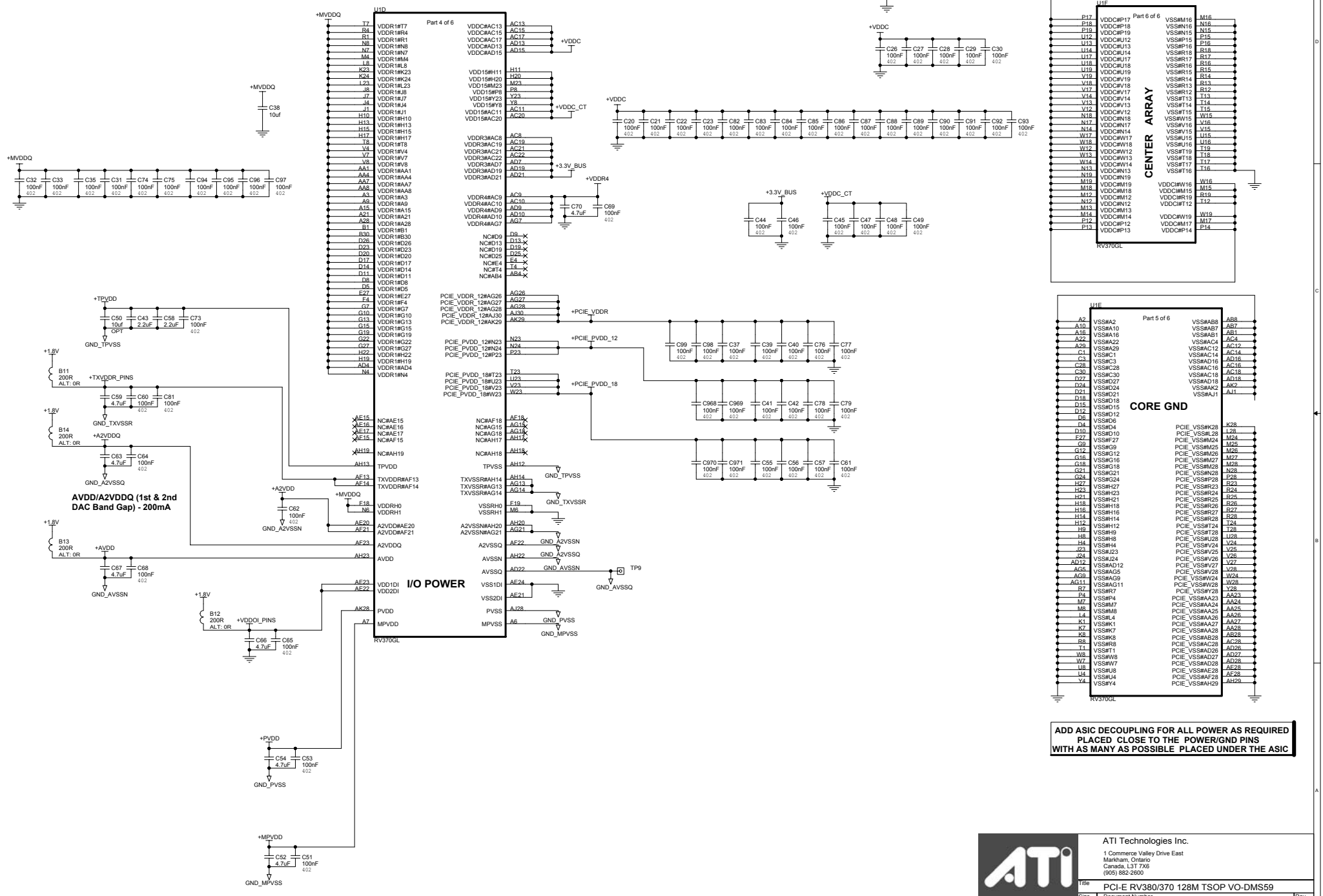
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS



VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT



Vout = 1.2V ~ 1.3V

ALT. 1: MAXIM REGULATOR

The schematic illustrates a power regulator circuit. Key components include:

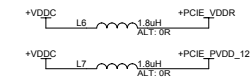
- Power Inputs:** +5V, +12V_BUS, and +PW_VDDC_HGD_R.
- MOSFET Driver Stage:** Two IRF7413A MOSFETs (Q24, Q22) are used to drive the high current path.
- High Current Path:** A B17 MOSFET (60R) handles the main load current from the +12V_BUS.
- Regulation and Feedback:** A feedback network consisting of resistors R351 (0R) and R352 (102) maintains regulation. A 0.8V reference (Ref) is provided by a precision resistor divider (R254, R383).
- Capacitors:** Various electrolytic and ceramic capacitors (C151, C149, C147, C148, C301, C322, C321, C323, C324) are used for decoupling and stability.
- Resistors:** Precision resistors (R314, R1247, R1248, R351, R352, R15, R254, R383) define the gain and reference voltage.

[illegible]

ISL6522CB : SOIC

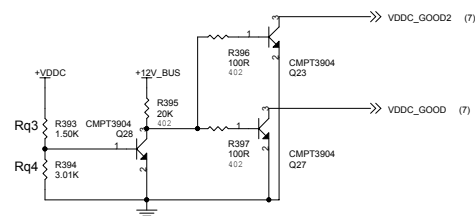
Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

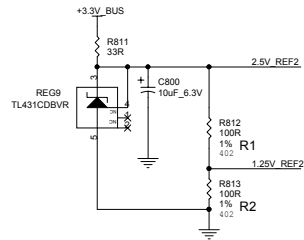
Part	Vout	R1	R2
MAX1954 ISL6522	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
0.8V Ref	1.25V	1.00K 1% ATI P/N 3240100100	1.78K 1% ATI P/N 3240178100
0.8V Ref	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100



Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K
+1.2V	1.5K	3K

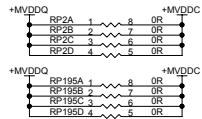




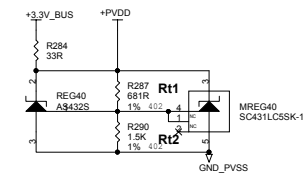
Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (402, 1%) P/N 3160200100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

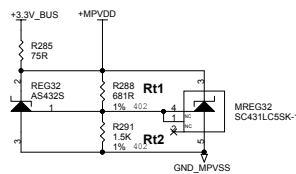
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	DNI P/N 3230000000 P/N 3150000000	DNI P/N 3150000000



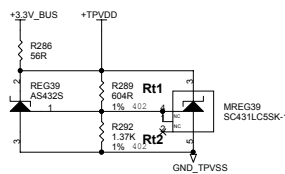
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



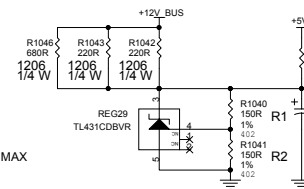
Alt. regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX

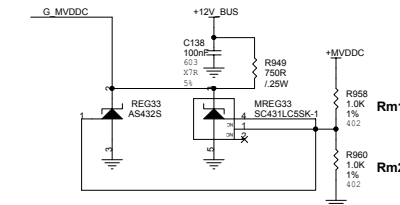


Alt regulator for +5V
Vout = 5V
Iout = 10mA MAX (+5V)



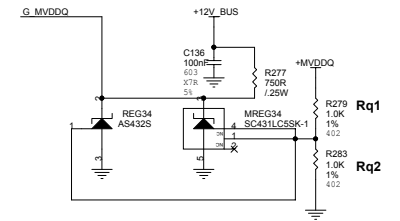
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100

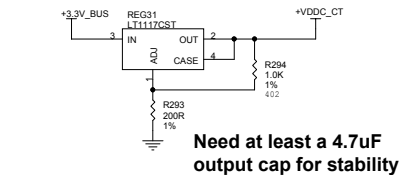


Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100



Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 150mA MAX

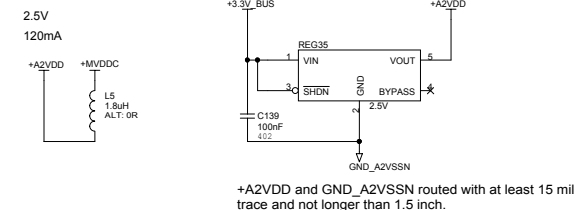


	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

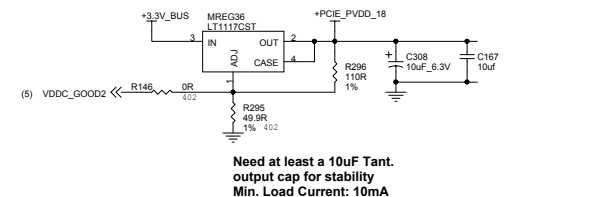
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada L3T 7X5
(905) 882-2600

Part No. **PCI-E RV380/370 128M TSOP VO-DMS59**
Size C Document Number **105-A259xx-00** Rev 3
Date: Thursday, July 15, 2004 Sheet 6 of 16

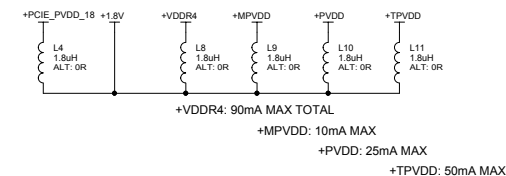
Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX



Alt. regulator for PCIE_PVDD_18
Vout = 1.82V
Iout = 500mA MAX

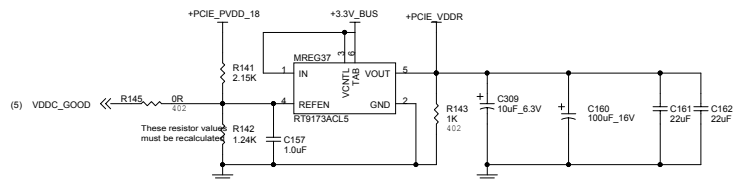


Optional when +Vout_Switcher is above 1.2V

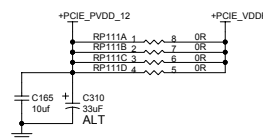


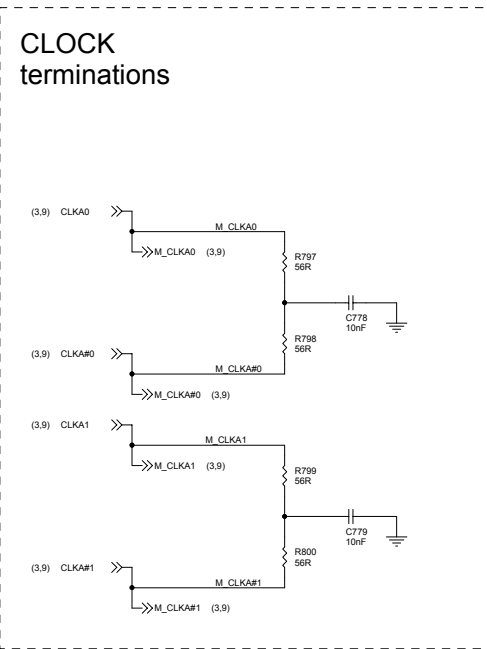
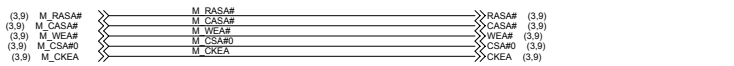
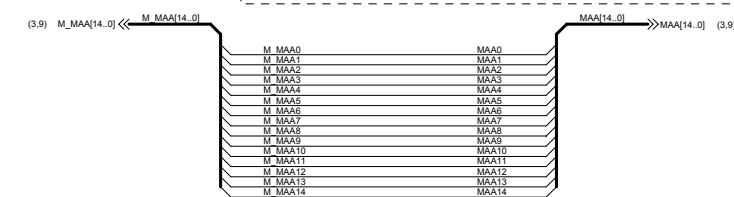
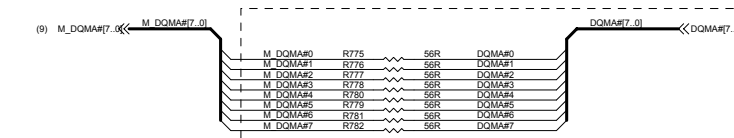
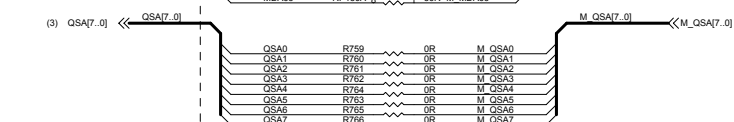
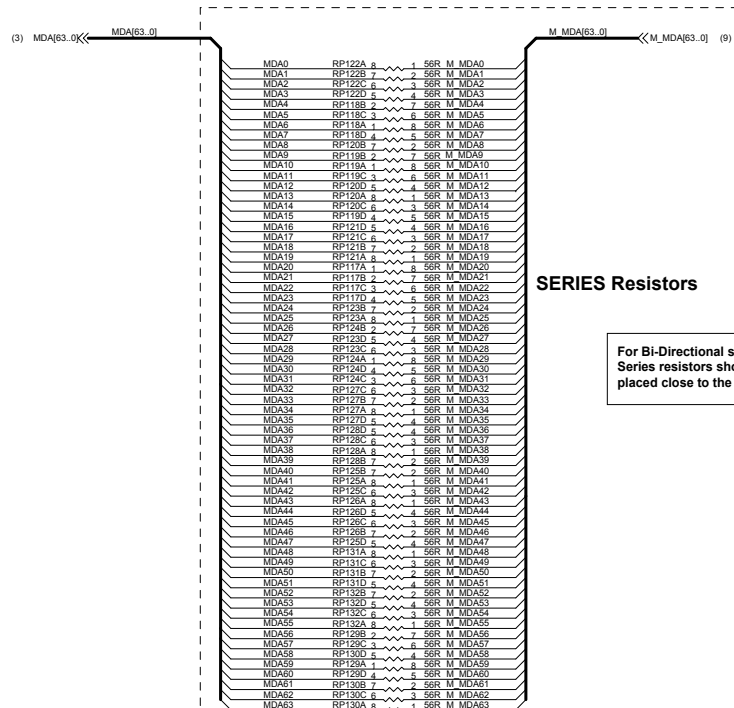
Rails derived from +VDDR4
 +AVDD: 10mA MAX
 +A2VDDQ: 20mA MAX
 +VDDO1_PINS: 20mA MAX
 +TXVDDR_PINS: 20mA MAX

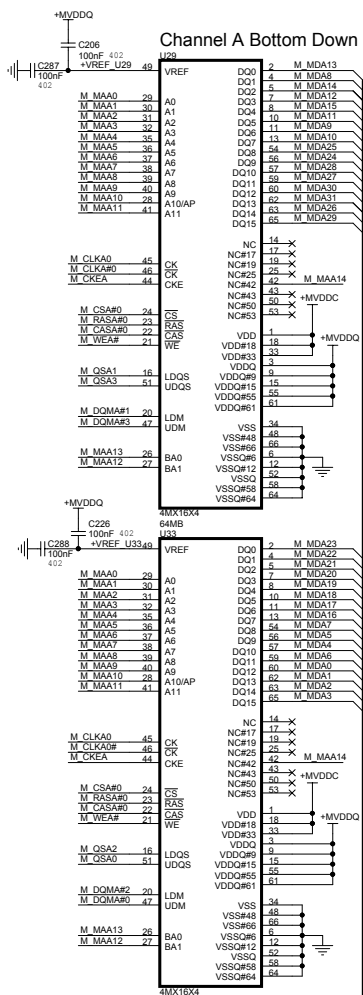
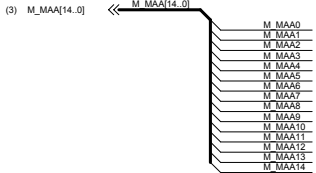
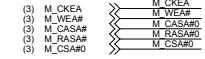
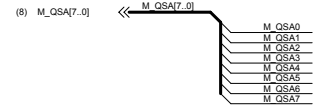
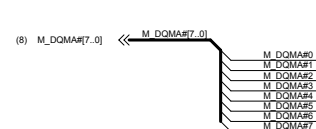
+PCIE_VDDR: 1.2V 1300mA MAX



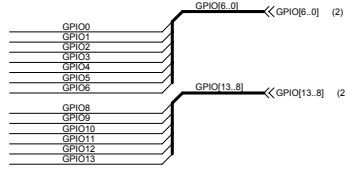
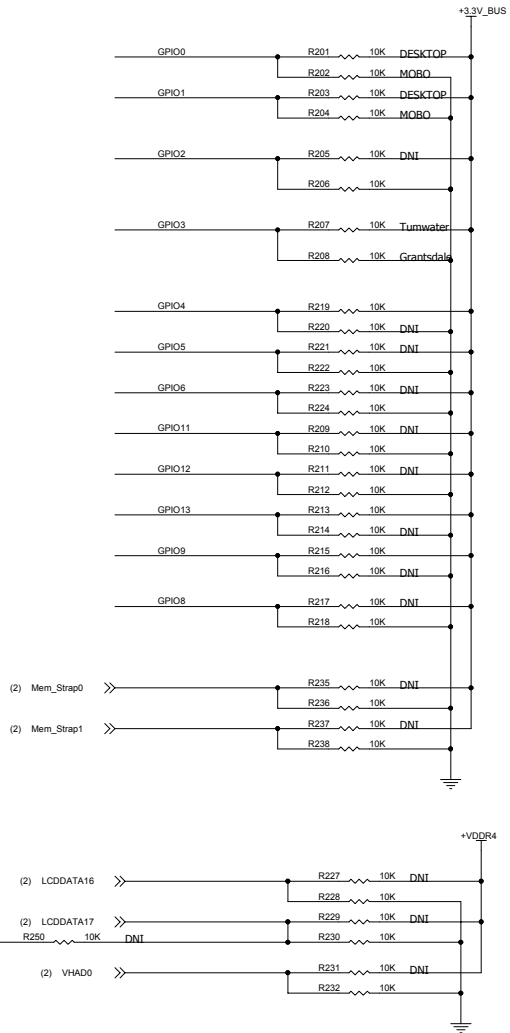
+PCIE_PVDD_12: 1.2V 250mA MAX







OPTION STRAPS

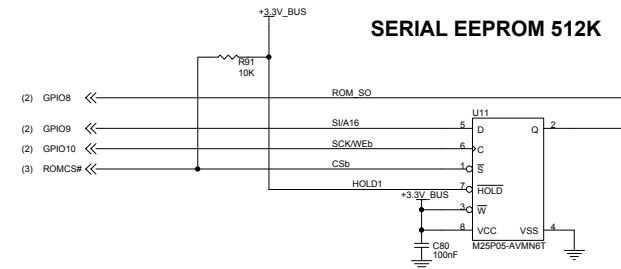


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_P_PLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45C08011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1101 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present. 1 - No slave VIP host port devices reporting presence during reset	

STRAP P	INTERRUPT
LOW	ENABLED (DEFAULT)
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	0	0
INF	1	0
HYN	0	1
ELPIDA	1	1

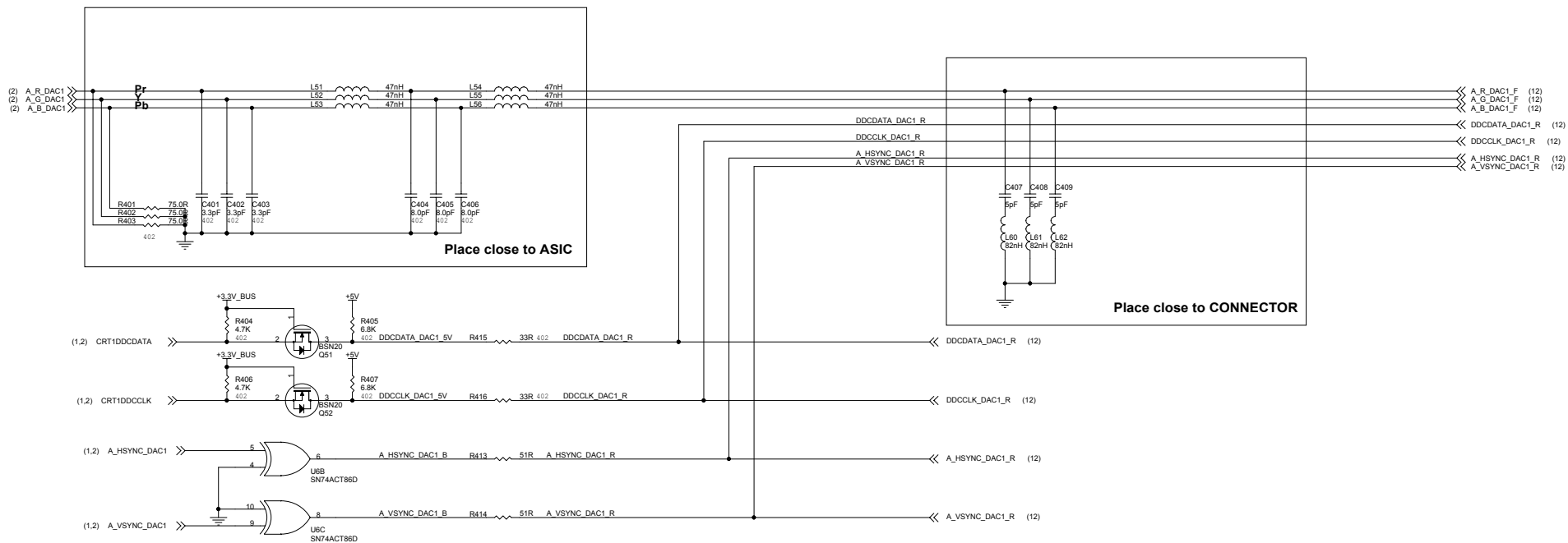
SERIAL EEPROM 512K



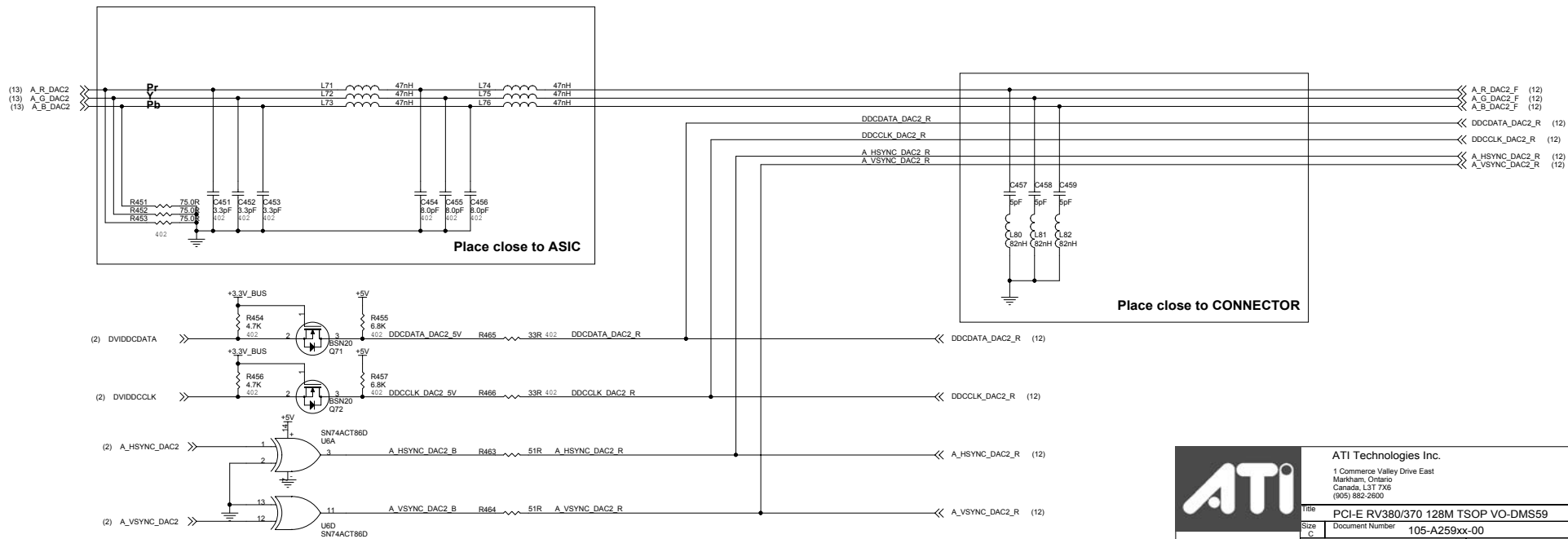
ATI Technologies Inc.
1 Commerce Valley Drive East
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Canada, L3T 7X5
(905) 882-2600

Doc Number: **PCI-E RV380/370 128M TSOP VO-DMS59**
Document Number: **105-A259xx-00**
Date: Thursday, July 15, 2004 Sheet 10 of 16 Rev 3

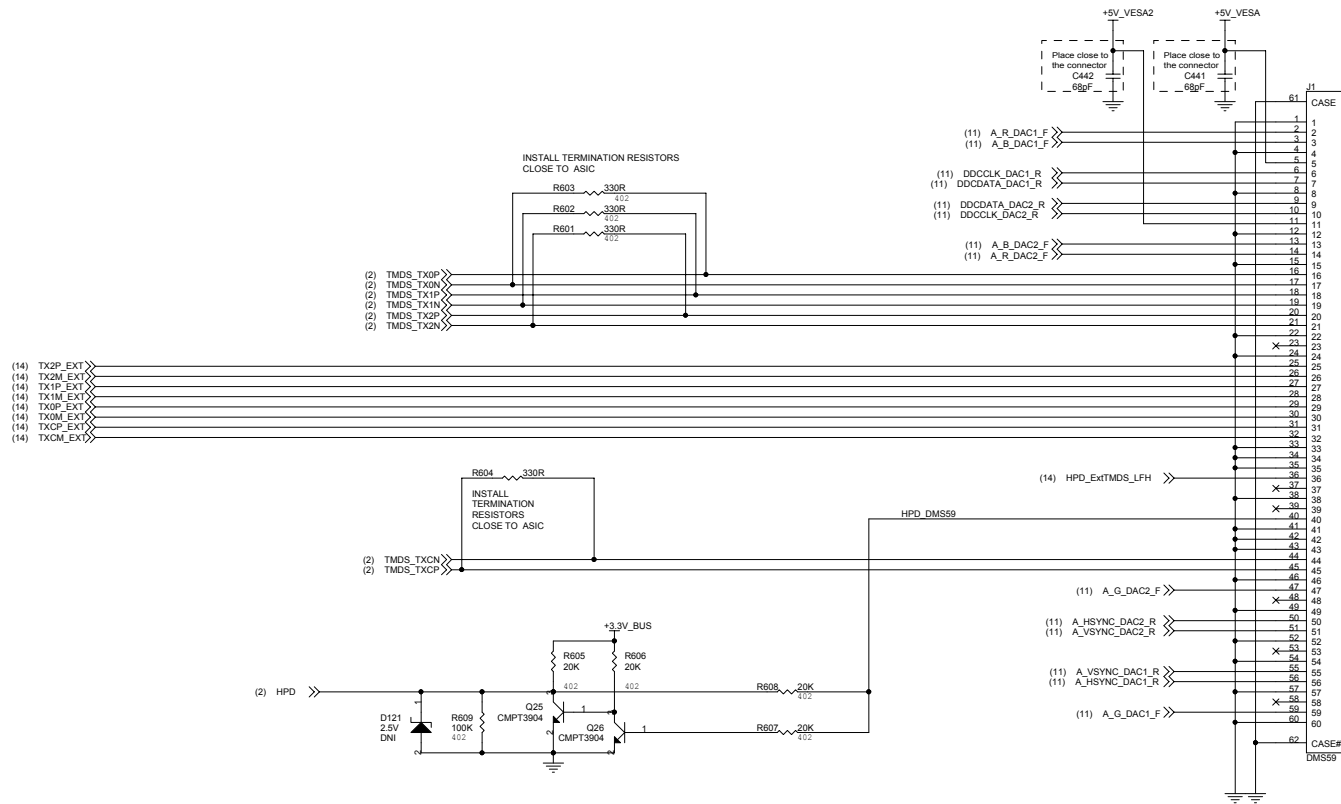
PRIMARY CRT



2nd CRT

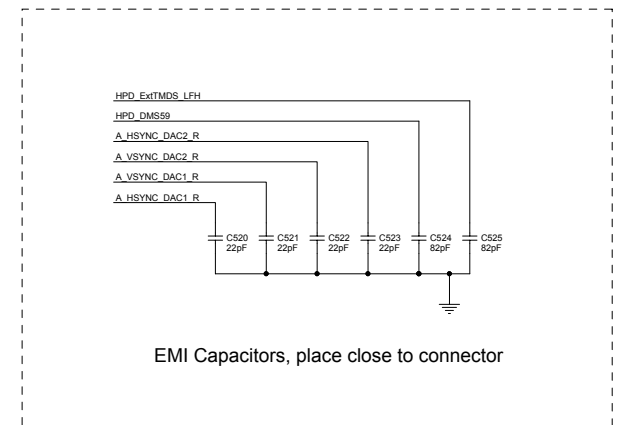
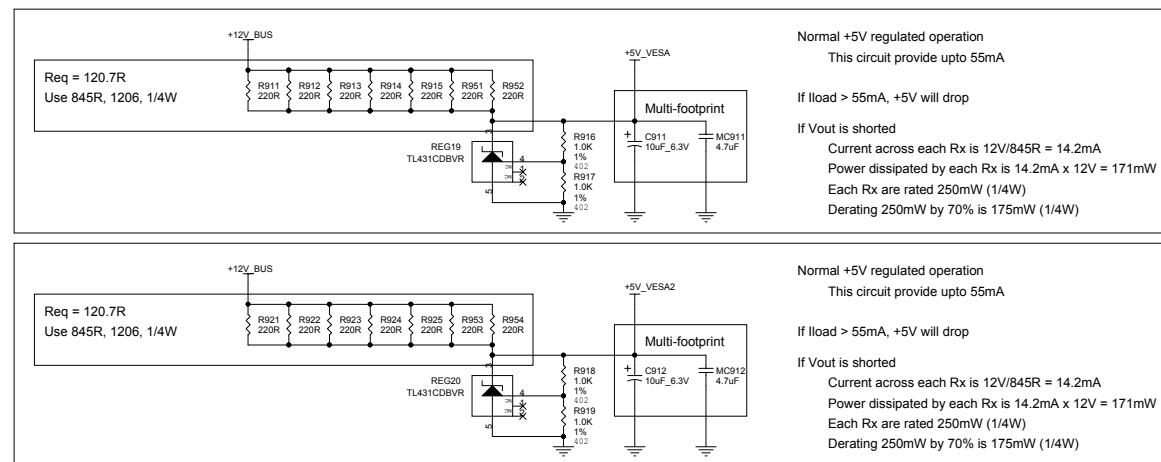


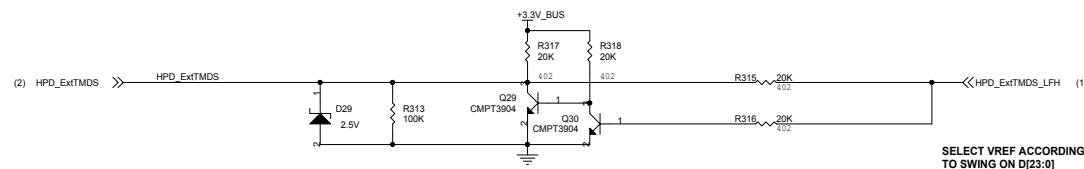
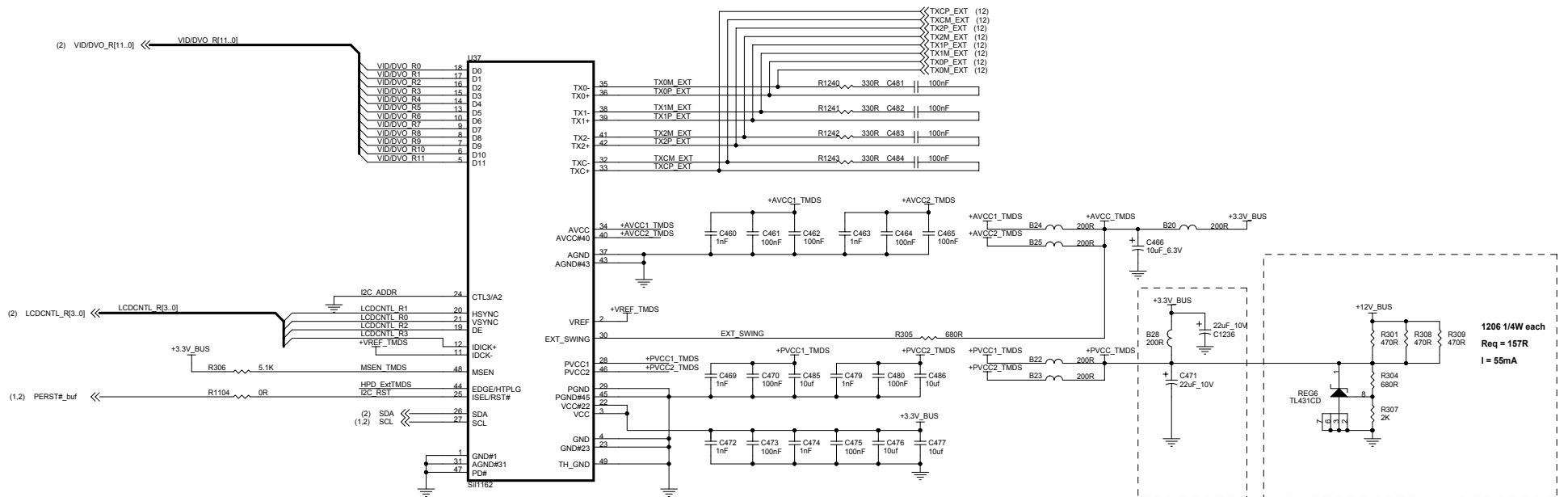
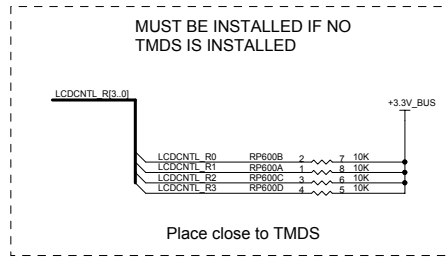
VESA Multi-Display Interface DMS-59 Connector



Connector 1	
Signals	Mapping
VGA:	DAC1
DVI:	External TMSD
HPD:	External TMSD HPD
DDC:	CRT1 DDC
5V:	+5V_VESA

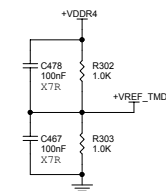
Connector 2	
Signals	Mapping
VGA:	DAC2 (TVDAC)
DVI:	Internal/Integrated TMSD
HPD:	Internal/Integrated TMSD HPD
DDC:	DVI DDC
5V:	+5V_VESA2





SELECT VREF ACCORDING
TO SWING ON D[23:0]

SELECT VREF ACCORDING
TO SWING ON D[23:0]



<Variant Name>

DVI/VGA SCREWS



SCREW



SCREW



SCREW
PAN_HEAD

MISC. BOARD PARTS



ANTISTATIC
BAG

6_X_11



BLANK
LABEL

1.5W_X_0.50H

9050005900;9050005900



ATI LOGO
LABEL

ATI_LOGO_LABEL



ATI LOGO
LABEL

MH101



HEATSINK
7120002700

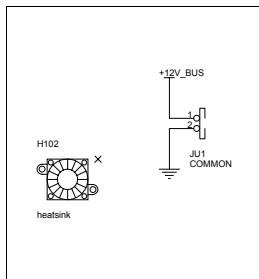
H101



HEATSINK
7120008000

MT1

MT_Hole_0.136_in.



LP brackets



BRACKET

LP, NO TABS, Dual DVI
8020032650



BRACKET

LP, TOP TAB, DIN, Dual DVI
8020032770

ATX brackets



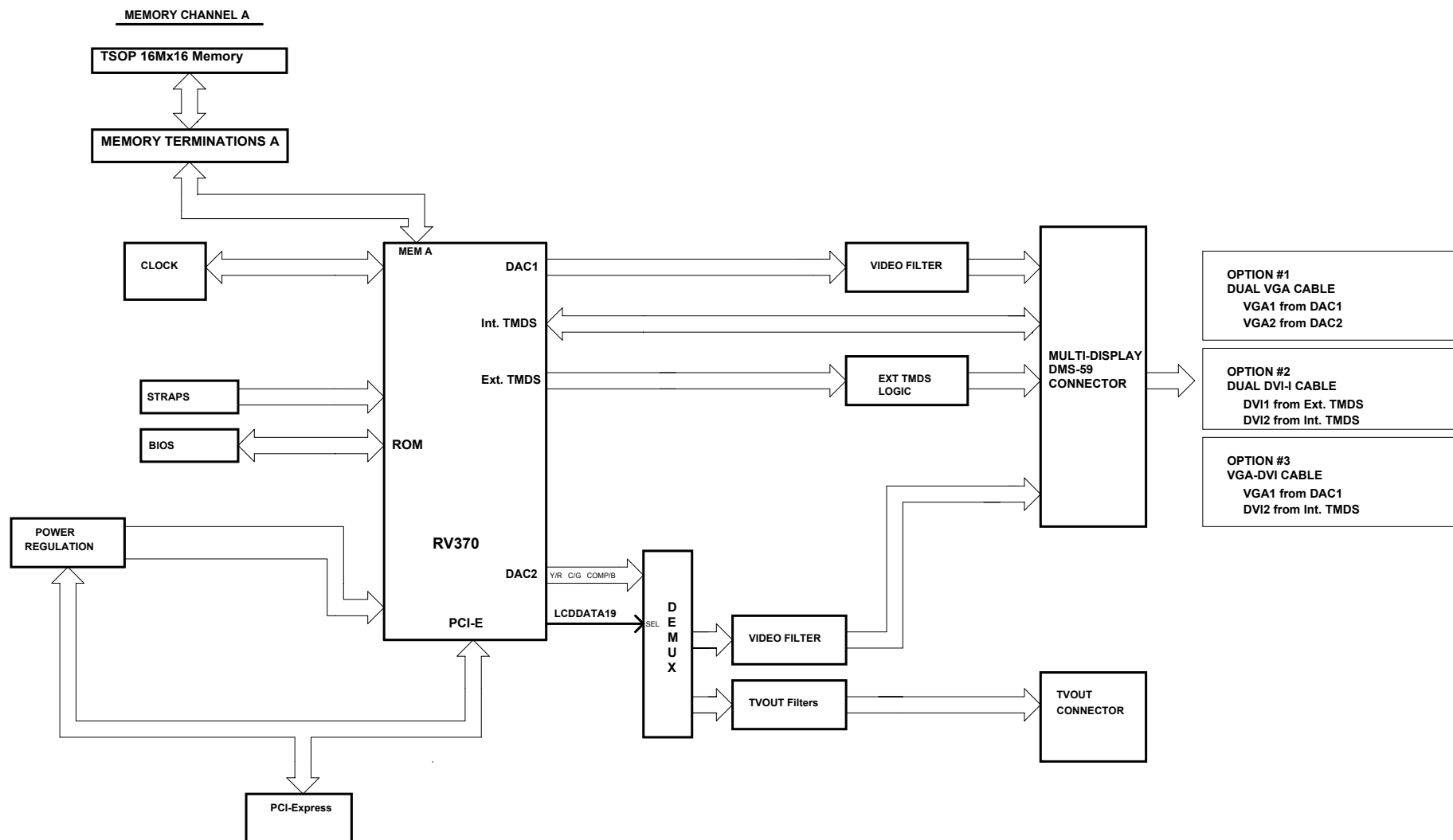
BRACKET

DUAL, NO TABS, Slim VGA, DIN, DVI



BRACKET

TOP TAB (LP), DIN, Dual DVI



<Variant Name>

REFERENCE DESIGN

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